IN THE CLAIMS

Claims 1-31. (Canceled)

32. (Previously presented) A semiconductor device comprising:

a plurality of inner leads extending around a semiconductor chip;

a thin sheet-shaped insulating member supporting said semiconductor chip and joined to an end portion of said respective inner leads;

a conductive wire for connecting surface electrodes of said semiconductor chip and said inner leads corresponding thereto;

a seal portion in which said semiconductor chip, said wire, and said insulating member are resin-sealed; and

a plurality of outer leads linked to said inner leads and exposed from said seal portion,

wherein an arrangement pitch of said surface electrodes of said semiconductor chip is 1/2 as much as or less than a minimum value of a tip pitch between said inner leads adjacent to each other.

33. (Canceled).

34. (Currently amended) The semiconductor device according to claim ~~31~~ 32, wherein said insulating member is a tape substrate.

35. (Currently amended) The semiconductor device according to claim ~~31~~ 32, wherein said insulating member is a glass-containing epoxy substrate.

36. (Currently amended) The semiconductor device according to claim ~~31~~ 32, wherein said semiconductor chip is mounted on a surface of an inner lead arrangement side of said insulating member.

37. (Currently amended) The semiconductor device according to claim ~~31~~ 32, wherein said inner leads and said insulating member are joined by an adhesive layer, and said semiconductor chip is thicker than a total of said insulating member and said adhesive layer in thickness.

38. (Currently amended) The semiconductor device according to claim ~~31~~ 32, wherein said insulating member and

said inner leads are joined by adhesive layers of a pressure sensitive adhesive double coated tape having a tape base, on both front and rear surfaces whose said adhesive layers are disposed.

39. (Currently amended) The semiconductor device according to claim ~~31~~ 32, wherein said inner leads and said insulating member are joined by an adhesive layer, and said adhesive layer is provided to connect the portion between said inner leads in an inner lead arrangement side of said insulating member.

40. (Currently amended) The semiconductor device according to claim ~~31~~ 32, wherein said inner leads and said insulating member are joined by an adhesive layer, and said adhesive layer is provided throughout the entirety of a surface of an inner lead arrangement side of said insulating member.

41. (Currently amended) The semiconductor device according to claim ~~31~~ 32, wherein said inner leads and said insulating member are joined by an adhesive layer, and said

adhesive layer is disposed just on an inner lead joining portion of said insulating member.

42. (Previously presented) The semiconductor device according to claim 35, wherein said glass-containing epoxy substrate contains alumina particles.

43. (Currently amended) A semiconductor device ~~comprising:~~ according to claim 32,

~~a semiconductor chip having a plurality of surface electrodes;~~

~~a conductive wire connected between a thin plate-shaped substrate supporting said semiconductor chip and said surface electrodes of said semiconductor chip;~~

~~a resin sealing portion having upper and lower surfaces and four side surfaces linked therebetween, and sealing said semiconductor chip, said wire, and said thin-plate shaped substrate; and~~

~~a plurality of leads each having a first portion connected to said surface electrodes of said semiconductor chip and said wire, and a second portion exposed from said resin sealing portion,~~

~~wherein each end of said plurality of leads and said thin plate shaped substrate are connected, and~~

~~wherein said second portions of said plurality of leads are respectively exposed along four sides of said lower surface of said resin sealing portion.~~

wherein a portion of said outer lead in each of a plurality of leads constituted by said inner leads and said outer leads is exposed along four sides of a lower surface of said seal portion and to said lower surface of said seal portion.